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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/955,926 | 09/18/2001 | Catherine Mallardeau | 00-GR1-374 | 9396 |

23334 7590 07/31/2003

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| EXAMINER | |
|---|---|
| MAGEE, THOMAS J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

A/70

| Office Action Summary | Application No. | Applicant(s) |
| --- | --- | --- |
| | 09/955,926 | MALLARDEAU ET AL. |
| | Examiner | Art Unit |
| | Thomas J. Magee | 2811 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for R ply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 22 April 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23, and 30 -34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Cancellations*

1. Applicant's cancellation of Claims 27 – 29 in Letter No. 10 of April 22, 2003 is acknowledged.

### *Claim Rejections – 35 U.S.C. 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, and 30 -32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. (US5,959,327) in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey (1993), pp. 157, 868).

4. Regarding Claims 1 and 2, Sandhu et al. disclose (Col. 4, lines 10 – 24) an integrated circuit with a plurality of active components (25) with junctions formed in the substrate with a passive component (capacitor) (Figure 13A) formed above the active components (25), further comprising a first insulating layer (40) separating the active components and the base of the passive component and a polysilicon plug (65) electrically connecting the passive component with an active component, wherein the terminal (plug) is formed in the thickness of the first insulating layer, having a lower surface of the terminal that contacts a junction of an active component and extends over a boundary of the junction of the active

component (Figure 13A) and onto an isolation region.

Sandhu et al. do not disclose the terminal to be composed of metal, but Wilson et al. disclose (p. 157, 868, $2^{nd}$ and $1^{st}$ para.) the use of tungsten as a notoriously well-known material used for plugs and interconnects. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

5. Regarding Claim 4, Sandhu et al. disclose (Col. 4, lines 34 – 38) that the surface of the first insulating layer (40) is planar, but do not disclose that the terminal is made of tungsten. Wilson et al. disclose (p. 157, 868, $2^{nd}$ and $1^{st}$ para.) the use of tungsten as a notoriously well-known material used for plugs and interconnects. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. to Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Further, Sandhu et al. do not explicitly disclose the thickness of the first insulating layer. However, in Figure 6, the polysilicon plug (65) is etched back 50 to 400 nm (0.05 to 0.4 um) (Col. 5, lines 12 – 17). Estimating from Figure 6, the thickness of the insulating layer (40) is 0.3 to 2.4 um, which is in the range recited in the instant application.

6. Regarding Claim 30, Sandhu et al. disclose (See Figure 13A) that the first insulating layer is a single layer (40) and the only insulating layer provided between passive component and active component.

7. Regarding Claim 31, Sandhu et al. disclose (See Figure 13A) that the base of the passive component (85) directly contacts the upper surface of the first insulating layer.

8. Regarding Claim 32, Sandhu et al. disclose areas of dielectric material (Col. 3, lines 60 – 67) (5, Figure 13A) for separating active components, wherein a portion of the lower terminal (65) contacts one of the areas of the dielectric material (5).

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al., as applied to Claims 1, 2, 4, 30, and 31, and further in view of Rhodes et al. (US 6,492,241 B1).

Sandhu et al. do not disclose the presence of a second insulating layer above the first. Rhodes et al. disclose (Col. 5, lines 16 – 22) a second insulating layer above the first with the passive component being set into a cavity formed throughout the second layer (110), Figure 1). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the secondary layer of Rhodes et al. in Sandhu et al. to obtain a completed device with an overlying protective dielectric.

Regarding second layer thickness, Rhodes et al. disclose (Col. 5, lines 29 – 31) that the thickness of the layer (110) is between 1.0 and 2.0 um, consistent with the 2.0 um value of the instant application. It has been ruled by the court that where the claimed ranges "overlap or lie inside ranges disclosed by the prior art," a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575,16 USPQ2d 1934 (Fed. Cir. 1990). Similarly, a prima facie case of

obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties.Titanium Metals Corp. of America v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985).

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al., as applied to Claims 1, 2, 4, 30, and 31 above, and further in view of Maeda (US 6,358,820 B1).

Sandhu et al. do not disclose that the passive component is an inductor. However, Maeda discloses (Col. 7, lines 3 – 17) an inductor (20) (Figure 1) within an insulating film (silicon oxide) formed on a first insulating structure (Figure 15) and electrically connected to a junction (14a1) through interconnects. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Maeda with Sandhu et al. and Wilson et al. to provide a means of incorporating an inductor on an insulating film above an active region, with reduced parasitic capacitance in an integrated circuit.

11. Claims 7 – 9, 11 – 13, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al. (p. 157, 868, 2nd and 1st para., 82 84), Sung et al. (US 6,133,599) and Trivedi (US 6,294, 464 B1).

12. Regarding Claims 7 and 8, Sandhu et al. disclose (Col. 4, lines 10 – 24) an integrated circuit including a plurality of transistors, passive components, and local connections formed within a first insulating layer deposited atop transistors of the integrated circuit. Sandhu

et al. do not disclose terminals to be composed of metal, but Wilson et al. disclose (p. 157, 868, 2nd and 1st para., 82 - 84) the use of tungsten and titanium (including reactants such as silicides) as a notoriously well-known materials used for plugs and interconnects. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Sandhu et al. disclose a plug (second terminal) (65 + 67 + 75) electrically connecting the passive component (that directly contacts the upper surface of the first insulating layer) with an active component, wherein the terminal (plug) passes completely through the thickness of the first insulating layer, having a lower surface of the terminal that contacts a junction of an active component and extends over a boundary of the junction of the active component (Figure 13A). As mentioned above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Sandhu et al. do not disclose the presence of a first metal terminal passing completely through the thickness of the first insulating layer, wherein the terminal constitutes a first stage of contact between an active area and a first level of interconnection. Sung et al. disclose (Col. 6, lines 43 – 44) the presence of a terminal plug (polysilicon) (first terminal) (17b, Figure 7) passing through the first insulating layer and contacting a tungsten plug (24, Figure 9) that is subsequently connected to an interconnect structure (26) (Col. 7,

lines 24 – 26). It would have then been obvious to one of ordinary skill in the art at the time of the invention to use the techniques of Sung et al. in Sandhu et al. to create a means for interconnecting areas of a DRAM cell. Further, as mentioned above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Additionally,Sandhu et al. do not disclose the presence of a third metal passing completely through the thickness of the first insulating layer, wherein the third metal horizontally connects two active areas of the integrated circuit. Trivedi discloses (Col. 8, lines 55 – 65) a metal layer (37) (Figure 7) connecting source/drain areas of two transistors. Further Trivedi discloses (Col. 9, lines 6 – 14) that additional interconnects may be formed utilizing additional metal (plugs) and an insulation layer, where the insulation layer would surround the third metal layer, wherein the third metal would pass through the insulating layer to contact the additional plug. It would then have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Trivedi in Sandhu et al. to obtain local interconnects that are required to provide the necessary electrical paths between transistors and other devices and external circuitry used to pass data to and from these devices (Trivedi, Col. 1, lines 19 – 23).

13. Regarding Claim 9, Sandhu et al. disclose (Col. 5, lines 5 – 11) that the passive component is a capacitor (See Figure 13A).

14. Regarding Claim 11, Sandhu et al. do not explicitly disclose the thickness of the first

insulating layer. However, in Figure 6, the polysilicon plug (65) is etched back 50 to 400 nm (0.05 to 0.4 um) (Col. 5, lines 12 – 17). Estimating from Figure 6, the thickness of the insulating layer (40) is 0.3 to 2.4 um, which is in the range recited in the instant application. Sandhu et al. also disclose that the top surface of the first insuating layer (40) is plane (Col. 4, lines 34 – 38). Sandhu et al. do not disclose that first, second, and third metal terminals are made principally of tungsten. Wilson et al. disclose (p. 157, 868, 2nd and 1st para.) tungsten as a notoriously well-known material used for plugs and interconnects. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

15. Regarding Claims 12 and 13, Sandhu et al. do not disclose the presence or thickness of a second insulating layer. Rhodes et al. disclose (Col. 5, lines 16 – 40) a second insulating layer (110) (Figure 1) above the first, wherein the passive component (120) rests on the first insulating layer and is formed throughout the second layer and the thickness is between about 1.0 and 2.0 um, consistent with the value recited in the instant application. It has been ruled by the court that where the claimed ranges "overlap or lie inside ranges disclosed by the prior art," a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575,16 USPQ2d 1934 (Fed. Cir. 1990). Similarly, a prima facie case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same

properties.Titanium Metals Corp. of America v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985).

16. Regarding Claim 33, Sandhu et al. disclose (See Figure 13A) that the first insulating layer is a single layer (40) and the only insulating layer provided between passive component and active component.

17. Regarding Claim 34, Sandhu et al. do not disclose that the third metal terminal is a local horizontal interconnection that directly connects two separate active areas. Trivedi discloses (Col. 8, lines 55 – 65) a metal layer (37) (Figure 7) connecting source/drain areas of two transistors. It would then have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Trivedi in Sandhu et al. to obtain local interconnects that are required to provide the necessary electrical paths between transistors and other devices and external circuitry used to pass data to and from these devices (Trevedi, Col. 1, lines 19 – 23).

18. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al., Sung et al., and Trivedi, as applied to Claims 7 – 9, 11 – 13, 33, and 34, and further in view of Maeda.

Sandhu et al. do not disclose that the passive component is an inductor. However, Maeda discloses (Col. 7, lines 3 – 17) an inductor (20) (Figure 1) within an insulating film (silicon oxide) formed on a first insulating structure (Figure 15) and electrically connected to a junction (14a1) through interconnects. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Maeda with Sandhu et al. and Wilson

et al. to provide a means of incorporating an inductor on an insulating film above an active region, with reduced parasitic capacitance in an integrated circuit.

19. Claims 14 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al. (pp. 157, 868, and 82 – 84) Sung et al., Rhodes et al., and Trivedi.

20. Regarding Claims 14 and 15, Sandhu et al. disclose an integrated circuit comprising: an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and storage capacitor (Col.4, lines 2 – 29)), a plurality of MOS transistors (Figure 13A) and a first insulating layer (40) separating transistors and base of storage capacitors.

Sandhu et al. do not disclose a first level of interconnection above the storage capacitors. However, Sung et al. disclose (Col. 7, lines 24 – 26) a first level of interconnection (26, Figure 9) positioned above storage capacitors. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to add Sung et al. to Sandhu et al. to provide a complete device with interconnections between active areas and external contact points.

Sandhu et al. do not disclose local interconnections including three terminals to be composed of metal, each opening onto each side of the first insulating layer. In the paragraphs to follow, positions of the "openings" are discussed in more detail. Wilson et al. disclose (p. 157, 868, 2nd and 1st para., 82 - 84) the use of tungsten and titanium (including reactants

such as silicides) as a notoriously well-known materials used for plugs and interconnects. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. to Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Sandhu et al. disclose a plug (second terminal) (65 + 67 + 85) electrically connecting one plate of the storage capacitor (that directly contacts the upper surface of the first insulating layer) with an active component, wherein the terminal (plug) passes completely through the thickness of the first insulating layer, having a lower surface of the terminal that contacts a junction of an active area and extends over a boundary of the junction of the active component (Figure 13A). As mentioned above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Sandhu et al. do not disclose the presence of a first metal terminal passing completely through the thickness of the first insulating layer, wherein the terminal constitutes a first stage of contact between an active area and a first level of interconnection. Sung et al. disclose (Col. 6, lines 43 – 44) the presence of a terminal plug (polysilicon) (first terminal) (17b, Figure 7) passing through the first insulating layer and contacting a tungsten plug (24, Figure 9) that is subsequently connected to an interconnect structure (26) (Col. 7, lines 24 – 26). It would have then been obvious to one of ordinary skill in the art at the

time of the invention to use the techniques of Sung et al. in Sandhu et al. to create a means for interconnecting areas of a DRAM cell. Further, as mentioned above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Additionally, Sandhu et al. do not disclose the presence of a third metal passing completely through the thickness of the first insulating layer, wherein the third metal horizontally connects two active areas of the integrated circuit. Trivedi discloses (Col. 8, lines 55 – 65) a metal layer (37) (Figure 7) connecting source/drain areas of two transistors. Further Trevedi discloses (Col. 9, lines 6 – 14) that additional interconnects may be formed utilizing additional metal (plugs) and an insulation layer, where the insulation layer would surround the third metal layer, wherein the third metal would pass through the insulating layer to contact the additional plug. It would then have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Trivedi in Sandhu et al. to obtain local interconnects that are required to provide the necessary electrical paths between transistors and other devices and external circuitry used to pass data to and from these devices (Trevedi, Col. 1, lines 19 – 23).

21. Regarding Claim 16, Sandhu et al. do not disclose the presence of a second insulating layer. However, Rhodes et al. disclose (Col. 5, lines 16 – 40) a second insulating layer (110, Figure 1) above the first (107) with a cavity (112) passing through the entire thickness of the second insulating layer and opening onto the top surface of the second

metal terminal, wherein the second metal terminal resides within the cavity and the top surface is on the cavity. Further, Rhodes et al. disclose that one plate of the storage capacitor (114) "carpets" the bottom and inside "flanks" of the cavity. It would, therefore have been obvious to one of ordinary skill in the art at the time of the invention to combine the secondary layer of Rhodes et al. in Sandhu et al. to obtain a completed device with an overlying protective dielectric.

22. Regarding Claim 17, Sandhu et al. do not disclose the presence of a third insulating layer above the second or a contact opening passing through the second and third insulating layers and contacting the first metal terminal. Trivedi discloses (Col. 9, lines 8 – 14) that additional processing may be done once a local interconnect (37) (Figure 7) is completed. This includes multiple insulation layers, and metal plugs and would include layers up to a third with a contact opening (Col. 10, lines 3 – 12) and contact made via a plug extending through layers to local metal interconnect. Hence it would be obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Trivedi in Sandhu et al. to obtain local interconnects that are required to provide the necessary electrical paths between transistors and other devices and external circuitry used to pass data to and from these devices (Trivedi, Col. 1, lines 19 – 23).

23. Regarding Claim 18, Sandhu et al. do not disclose that first, second, and third metal terminals are made principally of tungsten. Wilson et al. disclose (p. 157, 868, 2$^{nd}$ and 1$^{st}$ para.) tungsten as a notoriously well-known material used for plugs and interconnects. Hence, it would have been obvious to one of ordinary skill in the art at the time of the

invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

24. Claims 19 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. in view of Wilson et al., Sung et al., and Trivedi.

25. Regarding Claims 19 and 20, Sandhu et al. disclose an integrated circuit comprising: an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and storage capacitor (Col.4, lines 2 – 29)), a plurality of MOS transistors (Figure 13A) and a first insulating layer (40) separating transistors and base of storage capacitors.

Sandhu et al. do not disclose a first level of interconnection above the storage capacitors. However, Sung et al. disclose (Col. 7, lines 24 – 26) a first level of interconnection (26, Figure 9) positioned above storage capacitors. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to add Sung et al. to Sandhu et al. to provide a complete device with interconnections between active areas and external contact points.

Sandhu et al. do not disclose local interconnections including three terminals to be composed of metal, each opening onto each side of the first insulating layer. In the paragraphs to follow, positions of the "openings" are discussed in more detail. Wilson et al. disclose (p. 157, 868, 2nd and 1st para., 82 - 84) the use of tungsten and titanium (including reactants such as silicides) as a notoriously well-known materials used for plugs and interconnects.

Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. to Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Sandhu et al. disclose a plug (second terminal) (65 + 67 + 75 ) electrically connecting one plate of the storage capacitor (that directly contacts the upper surface of the first insulating layer) with an active component, wherein the terminal (plug) passes completely through the thickness of the first insulating layer, having a lower surface of the terminal that contacts a junction of an active area and extends over a boundary of the junction of the active component (Figure 8). As mentioned above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Sandhu et al. do not disclose the presence of a first metal terminal passing completely through the thickness of the first insulating layer, wherein the terminal constitutes a first stage of contact between an active area and a first level of interconnection. Sung et al. disclose (Col. 6, lines 43 – 44) the presence of a terminal plug (polysilicon) (first terminal) (17b, Figure 7) passing through the first insulating layer and contacting a tungsten plug (24, Figure 9) that is subsequently connected to an interconnect structure (26) (Col. 7, lines 24 – 26). It would have then been obvious to one of ordinary skill in the art at the time of the invention to use the techniques of Sung et al. in Sandhu et al. to create a means for interconnecting areas of a DRAM cell. Further, as mentioned above, it would

have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

Additionally, Sandhu et al. do not disclose the presence of a third metal passing completely through the thickness of the first insulating layer, wherein the third metal horizontally connects two active areas of the integrated circuit. Trivedi discloses (Col. 8, lines 55 – 65) a metal layer (37) (Figure 7) connecting source/drain areas of two transistors. Further Trevedi discloses (Col. 9, lines 6 – 14) that additional interconnects may be formed utilizing additional metal (plugs) and an insulation layer, where the insulation layer would surround the third metal layer, wherein the third metal would pass through the insulating layer to contact the additional plug. It would then have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Trivedi in Sandhu et al. to obtain local interconnects that are required to provide the necessary electrical paths between transistors and other devices and external circuitry used to pass data to and from these devices (Trivedi, Col. 1, lines 19 – 23).

26. Regarding Claim 21, Sandhu et al. do not disclose the presence of a second insulating layer above the first in a device within an integrated circuit. Rhodes et al. disclose (Col. 5, lines 16 – 40) a second insulating layer (110, Figure 1) above the first (107) with a cavity (112) passing through the entire thickness of the second insulating layer and opening onto the top surface of the second metal terminal, wherein the second metal terminal resides within the cavity and the top surface is on the cavity. Further, Rhodes et al. disclose that

one plate of the storage capacitor (114) "carpets" the bottom and inside "flanks" of the cavity. It would, therefore have been obvious to one of ordinary skill in the art at the time of the invention to combine the secondary layer of Rhodes et al. in Sandhu et al. to obtain a completed device with an overlying protective dielectric.

27. Regarding Claim 22, Sandhu et al. do not disclose the presence of a third insulating layer above the second or a contact opening passing through the second and third insulating layers and contacting the first metal terminal. Trivedi discloses (Col. 9, lines 8 – 14) that additional processing may be done once a local interconnect (37) (Figure 7) is completed. This includes multiple insulation layers, and metal plugs and would include layers up to a third with a contact opening (Col. 10, lines 3 – 12) and contact made via a plug extending through layers to local metal interconnect. Hence it would be obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Trevedi in Sandhu et al. to obtain local interconnects that are required to provide the necessary electrical paths between transistors and other devices and external circuitry used to pass data to and from these devices (Trivedi, Col. 1, lines 19 – 23).

28. Regarding Claim 23, Sandhu et al. do not disclose that first, second, and third metal terminals are made principally of tungsten. Wilson et al. disclose (p. 157, 868, 2$^{nd}$ and 1$^{st}$ para.) tungsten as a notoriously well-known material used for plugs and interconnects. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Sandhu et al. to obtain process-stable metal plugs connecting active and passive components of the circuit.

### ***Response to Arguments***

29. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305**

**5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Thomas Magee
July 6, 2003

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800